A HIGH PERFORMANCE 2-18.5 GHz DISTRIBUTED AMPLIFIER, THEORY AND EXPERIMENT

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ABSTRACT

A high performance 2-18.5 GHz monolithic GaAs MESFET distributed amplifier has been designed and fabricated. The m-derived drain line design is analyzed theoretically and a closed form gain equation is presented. Theoretical predictions are compared to measured results and more complicated CAD models. The measured small signal gain is typically 8.0 ± 0.25dB from 2-18.5 GHz at standard bias. Typical input return loss is greater than 12dB and the output return loss is greater than 15dB. The saturated output power is in excess of 23dBm over most of the band and the noise figure is less than 7.5dB.

INTRODUCTION

The distributed amplifier is based on the principles of the artificial transmission line. Zobel[1] first formalized the theory of these networks in 1924 using iterative impedance and propagation functions. The idea of absorbing the input and output capacitance of an active device into artificial transmission lines was first implemented in vacuum tube amplifiers by Percival[2] and later by Ginzton, et al[3]. The MESFET distributed amplifier has received much attention because of its extreme broadband behavior and relative ease of realization in monolithic form.

Experimental results have been published for GaAs MMIC distributed amplifiers using m-derived drain topology[4-6]. As far as this author knows, a gain expression for the m-derived MMIC distributed amplifier has not been provided. The theory included in this paper leads to an expression for the gain of a monolithic distributed amplifier with an m-derived drain line taking into account the capacitance associated with transmission-line inductors.

THEORY

A formulation for the distributed amplifier network using a normalized transmission matrix is presented in this paper. As far as this author knows, this is a new approach. This method can be applied to the coupled, nonuniform, constant-k case, as well as the m-derived case. The approach is general and provides good insight into the operation of the distributed amplifier.

In order to analyze the distributed amplifier with artificial transmission line techniques, a substitution of pi equivalents for microstrip lines is convenient. Typical designs will have relatively short microstrip lengths, so that over most of the passband, the L's and C's of the pi equivalents are essentially constant. When necessary, frequency dependence can be readily included. Loss in the microstrip lines can be accounted for by associating finite Q with the elements.

By normalizing the signals on the gate and drain lines to the characteristic impedance of the lumped lines and then writing a transmission matrix for the four-port unit cell, it is possible to arrive at a simple expression for the signals on the gate and drain lines. This matrix equation will be reduced to an expression for S_{21} of the m-derived case.

Consider the case of a voltage dependent current source connected in parallel across a transmission line of characteristic impedance, Z_{ob}. Normalizing the signals on the lines using the scattering formalism (see Fig. 1),

$$b_n^{\pm} = \frac{V_{bn}}{\sqrt{Z_{ob}}} \pm i_{bn}\sqrt{Z_{ob}}$$

$$a_n^{\pm} = \frac{V_{an}}{\sqrt{Z_{oa}}} \pm i_{an}\sqrt{Z_{oa}}$$

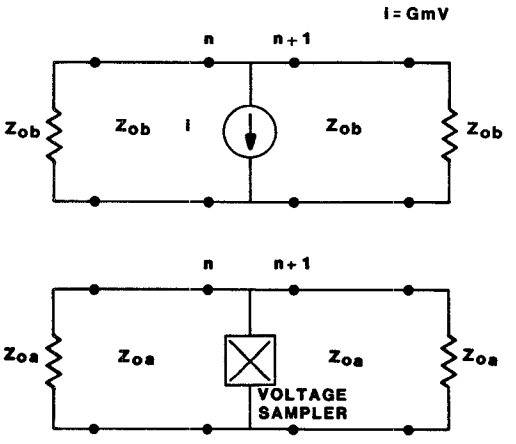

Figure 1. Generalized Distributed Amplifier Section

Since the current will split equally in both directions, we have

$$b_n^- = b_{n+1}^+ = -i/2\sqrt{Z_{ob}} \qquad (1)$$

$$i = g_m V_{an} \frac{1}{1+jw/wg}, \quad w_g = \frac{1}{R_g C_g}$$

Clearly,

$$b_{n+1}^+ = \frac{-g_m\sqrt{Z_{oa}Z_{ob}}}{2(1+jw/wg)}(a_n^+ + a_n^-)$$

$$a_n^\pm = a_{n+1}^\pm$$

Incident signals on the drain line will superimpose on those signals generated at the controlled source, such that

$$b_{n+1}^+ = H(a_n^+ + a_n^-) + b_n^+$$

$$b_n^- = H(a_n^+ + a_n^-) + b_{n+1}^-$$

where $H = -\frac{1}{2}g_m\sqrt{Z_{oa}Z_{ob}}(1+jw/wg)^{-1}$

Using the normalized transmission matrix formalism,

$$\underline{w}_{n+1} = \begin{bmatrix} 1 & 0 & 0 & 0 \\ H & 1 & H & 0 \\ 0 & 0 & 1 & 0 \\ -H & 0 & -H & 1 \end{bmatrix} \underline{w}_n$$

where,

$$\underline{w}_n = \begin{bmatrix} a_n^+ \\ b_n^+ \\ a_n^- \\ b_n^- \end{bmatrix}$$

The gate line is matched, so $a_n^- = 0$. If the drain line is matched, we need only consider incident signals, b_i^+.

$$\begin{bmatrix} b_{n+1}^+ \\ a_{n+1}^+ \end{bmatrix} = e^{-\theta_o} \begin{bmatrix} e^{\theta_d} & He^{\theta_d} \\ 0 & e^{-\theta_d} \end{bmatrix} \begin{bmatrix} b_n^+ \\ a_n^+ \end{bmatrix} \qquad (2)$$

where

$$\theta_o = \frac{\theta_a + \theta_b}{2} \qquad \theta_d = \frac{\theta_a - \theta_b}{2}$$

and θ_a & θ_b are the propagation functions of the gate and drain lines, respectively.

The matrix of Eq. 2 has the eigenvalues e^{θ_d} and $e^{-\theta_d}$ and associated eigenvectors

$$\begin{bmatrix} b_{e1} \\ a_{e1} \end{bmatrix} = a_o \begin{bmatrix} \frac{-He^{\theta_d}}{2\sinh\theta_d} \\ 0 \end{bmatrix}, \quad \begin{bmatrix} b_{e2} \\ a_{e2} \end{bmatrix} = a_o \begin{bmatrix} \frac{He^{\theta_d}}{2\sinh\theta_d} \\ 1 \end{bmatrix}$$

where a_o is an arbitrary constant.

The signal at the output of N sections is given by,

$$b_N^+ = (\lambda_{e_1}^N b_{e1} + \lambda_{e_2}^N b_{e2})e^{-N\theta_o}$$

or

$$\frac{b_N^+}{a_o} = \frac{H\sinh N\theta_d}{\sinh\theta_d} e^{-N\theta_o e^{\theta_d}} \qquad (3)$$

Equation 3 relates the incident gate signal at the first gate to the incident drain signal at the output of the last full section of the drain line. Typically, the gate line is driven one half-section before the first gate, and the drain line output is taken one half-section from the last drain. Therefore, multiplying Eq. 2 by $e^{-\theta_d}$ yields an expression for S_{21}.

$$S_{21} = \frac{b_n^+}{a_o} = \frac{H\sinh N\theta_d}{\sinh\theta_d} e^{-N\theta_o} \qquad (4)$$

Note that Z_{oa} and Z_{ob} must be replaced by $Z_{\pi g}$ and $Z_{\pi d}$, the pi impedances of the gate and drain lines in the equation for H.

Equation 4 is exact under the following assumptions:

1. Unilateral FET
2. Perfect match at gate and drain lines

To arrive at the m-derived case, we need to transform the circuit to the case covered by Eq. 4. The circuit we desire to analyze is shown in Fig. 2.

Computing a Thevinen and then a Norton equivalent, the drain circuit is simplified to that of Fig. 3, where

$$i' = \frac{i}{1+\alpha(jw/w_{Ld} - 4w^2/w_{cd}^2)}$$

$$w_{cd} = \frac{2}{\sqrt{L_d C_d}}, \quad w_{Ld} = \frac{1}{\sqrt{G_d L_d}}$$

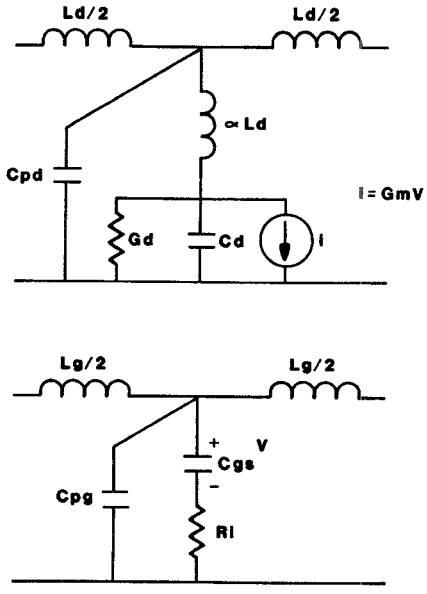

Figure 2. M-derived Drain Line Distributed Amplifier Section As Realized in an MMIC

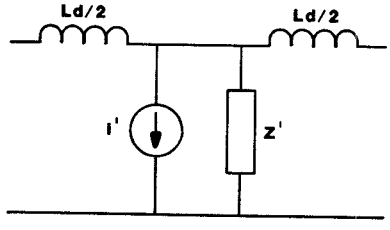

Figure 3. Transformed m-derived Drain Line Section

Substituting i' for i in Eq. 1, results in a new expression for H:

$$H = \frac{-g_m \sqrt{Z_{\pi g} Z_{\pi d}}}{2(1+jw/w_g)\,(1+\alpha((jw/w_{Ld}-4w^2/w^2_{cd}))} \qquad (5)$$

The pi-section characteristic impedance of the drain line is computed using Z' from Fig. 3.

GAIN CALCULATIONS

The amplifier was modeled on the SuperCompact circuit analysis program in order to take into account coupling between the elements and microstrip discontinuities.

Equation (4) is evaluated using lumped elements determined from y-parameters of the microstrip inductors as modeled on SuperCompact. Transistor R_g, C_{gs}, R_d and C_{ds} were determined from a more complicated model, which was derived from DC and RF measurements. The CAD model and the analytical expression are compared in Fig. 4. The analytic expression tends to be optimistic by a maximum of 2.1dB. Apparently, the assumptions made in Eq. 4, namely perfect match at all four ports and zero gate-drain capacitance, have a significant effect. Omissions such as microstrip loss, frequency dependence of elements are probably second order, but can be taken into account in Eq. 4.

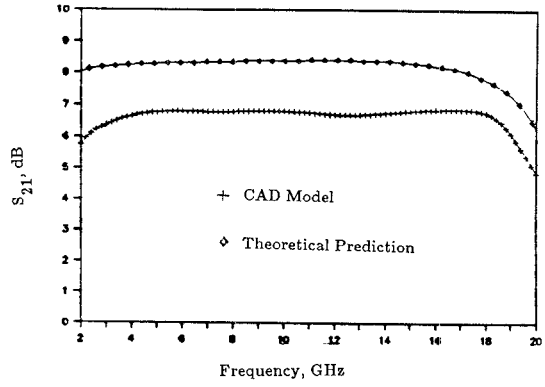

Figure 4. Theoretical vs. More Complicated CAD Model

DEVICE FABRICATION

The active layer on the GaAs wafers was prepared using ion implantation directly into low chromium doped LEC substrates. Device isolation was achieved using mesa etching. This step also defines the GaAs resistors used on the MMIC. Ohmic contacts were fabricated using alloyed AuGe\NiAu. Electron beam lithography was used to define 0.5 um gates (all other steps use conventional contact photolithography). The gates were recessed and then metallized using TiPtAu.

A TiAu pattern was defined, forming overlay metal, bonding pads, lower capacitor plates, and transmission lines. A dielectric consisting of 2000 Å of silicon nitride was applied using plasma enhanced chemical vapor deposition, and then patterned. The silicon nitride serves as the capacitor dielectric and also protects the gate areas of the FETs. Capacitor top plates were formed using TiAu.

The wafers were plated using the conventional two-resist approach that allows formation of air bridges. These air bridges are used to interconnect FET source pads and to connect top capacitor plates to adjacent metallization. Bond pads, transmission lines, and top capacitor plates are also plated during this step. This completes frontside processing.

The wafers were then mounted to a glass substrate for backside processing. The wafers were lapped to 0.006 inches. Then resist was spun on the back of the slice and the via hole pattern exposed, using an infrared aligner to align this pattern to the frontside metallization. Reactive ion etching was then used to form the via holes. The backside was then metallized and plated. The wafers were transferred to a stretchable tape for sawing and expanding.

EXPERIMENTAL RESULTS

A picture of the amplifier is shown in Fig. 5. The device measures 0.093 x 0.064 inches. Bias current is fed into the drain line through a large spiral inductor, shunting the resistive drain termination. The gate bias is applied through the gate terminating resistor. Both points are bypassed to ground through capacitors connected to via holes. The active elements are four 189um x 0.5um interdigital MESFETs.

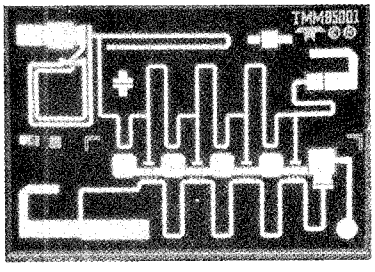

Figure 5. TMM85001 Distributed Amplifier

Measured results of gain and return loss from several devices are shown in Figs. 6, 7, and 8. Saturated output power and one dB compressed power are shown in Fig. 9. A typical noise figure plot appears in Fig. 10.

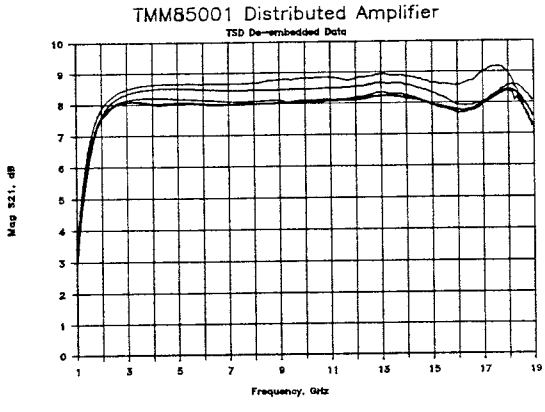

Figure 6. Measured Gain

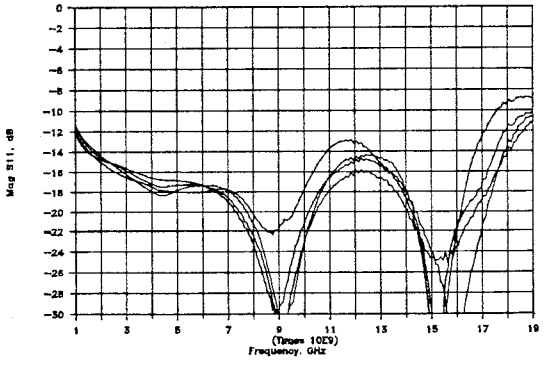

Figure 7. Measured Input Return Loss

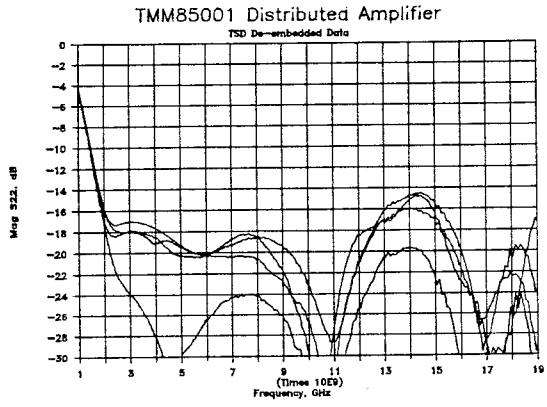

Figure 8. Measured Output Return Loss

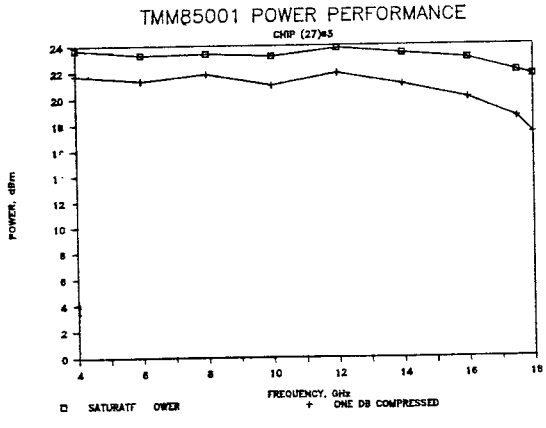

Figure 9. Measured Output Power

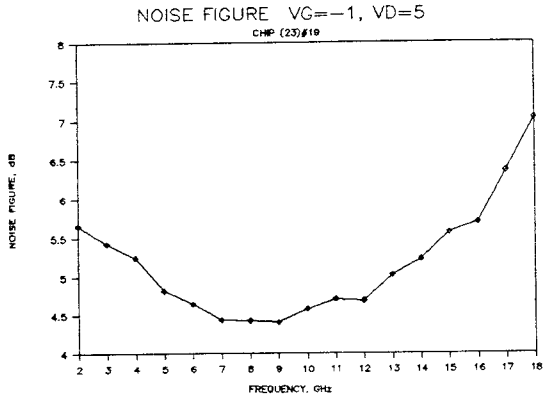

Figure 10. Measured Noise Figure

While designed primarily as a small gain signal stage, the amplifier performs well in terms of output power and noise figure. There were initial problems cascading these devices, however, when placed in an evanescent waveguide, a three-stage cascade provided gain of 22dB $\pm$0.75dB.

The experimental gain results are clearly much higher than modeled. This is mostly due to high transconductance.

CONCLUSION

Theoretical results using a new formulation for the distributed amplifier have been presented. A gain expression for the commonly used m-derived topology has been derived. The expression is compared to a complicated SuperCompact model and is seen to be optimistic by approximately 23% at midband. The error is probably due primarily to the unilateral assumption and imperfect terminations.

Experimental results show excellent gain and return loss over 2-18.5 GHz.

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BIBLIOGRAPHY

1. O.J. Zobel, "Theory and Design of Composite Wave-Filters", Bell system Technical Journal, 3, 1924, p567

2. W.S. Percival, British Patent Specification No. 460 562, July 24, 1936

3. E.L. Ginzton, W.R. Hewlett, J.H. Jasburg, and J.D. Noe, "Distributed Amplification", Proc. IRE, vol. 36, pp 956-969, 1948

4. W. Kennan, T. Andrade, and C.C. Huang, "A 2-18 GHz Monolithic Distributed Amplifier Using Dual-Gate GaAs FETs", IEEE Transactions on Microwave Theory and Tech., vol. MTT-32, No.12, Dec. 1984

5. R. Pauley, P. Asher, J. Schellenberg, and H. Yamasaki, A 2-40 GHz Monolithic Distributed Amplifier", IEEE Gallium Arsenide Integrated Circuits Symposium Technical Digest, Nov. 12-24, 1985.

6. Y. Ayasli, S.W. Miller, R. Mozzi, and L.K. Hanes, "Capacitively Coupled Traveling-Wave Power Amplifier", IEEE Transactions in Microwave Theory and Tech. vol MTT-32, No. 12, Dec. 1984